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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,458	12/05/2003	Yi Song Chiu	N1085-90156	1305

8933 7590 09/25/2006

DUANE MORRIS, LLP  
IP DEPARTMENT  
30 SOUTH 17TH STREET  
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EXAMINER

DAHIMENE, MAHMOUD

ART UNIT PAPER NUMBER

1765

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action  
Before the Filing of an Appeal Brief**

Application No.

10/729,458

Applicant(s)

CHIU ET AL.

Examiner

Mahmoud Dahimene

Art Unit

1765

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 08 September 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 1-30.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

NADINE G. NORTON  
SUPERVISORY PATENT EXAMINER

*N.*

Continuation of 11. does NOT place the application in condition for allowance because: Regarding the amendment in claim 1 of removing photoresist "while" forming a second insulator layer, Lim et al. (US 2005/0093063)(the primary reference cited in the last office action mailed on 7/13/2006) cites "The ashing removes patterned masking layer 16 and also results in the growth of additional dielectric 22 at the surface of substrate 12." (page 2, paragraph 0020). As to the amendment regarding forming a first conductive structure on said first gate insulator layer and a second conductive gate structure on said second gate insulator layer' Lim does show conductive layers (38) and (50) on the gate insulator layers for both regions (figure 6).

As to the argument that Lim teaches away from exposing the bare Si substrate surface because a rough surface will result. As stated in the last office action, the examiner maintains that it would have been obvious to one of ordinary skill in the art at the time the invention was made, willing to accept a silicon rough surface after etch and pre-clean, to modify the process of Lim to remove completely the dielectric (14) in region (8) to expose a bare substrate in region (8) because the reference of Lim et al. suggests it is conventional to remove all the dielectric in the instance where a rougher surface of the substrate is acceptable. One of ordinary skill in the art would have been motivated to completely remove the dielectric in region (8) in order to grow a second dielectric in region (8) with a different thickness than the first dielectric of region (6). Lim provides an improvement to the method of forming multiple gate structures where a smoother surface of the silicon substrate is required. One of ordinary skill in the art seeking to form multiple gate structures where a smoother surface of the silicon substrate is not required would have found it obvious to modify the method of Lim by using the conventional step of removing all the oxide to a bare Si surface because this step is simpler to implement since in such a case a conventional endpoint detection system can be used to stop the oxide removal step, while a partial oxide removal step is harder to implement since removal endpoint detection cannot be used. Lim does not teach away from removing all the oxide in the second region for all applications, Lim merely proposes an improvement of a method when a smoother silicon surface is required.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.